

1 ABSTRACT OF THE DISCLOSURE

2 The invention includes a method for forming graded junction
3 regions comprising: a) providing a semiconductor material wafer; b)
4 providing a transistor gate over the semiconductor material wafer, the
5 transistor gate having opposing lateral sidewalls; c) providing sidewall
6 spacers adjacent the sidewalls of the transistor gate, the sidewall spacers
7 having a lateral thickness; d) decreasing the lateral thickness of the
8 sidewall spacers; and e) after decreasing the lateral thickness of the
9 sidewall spacers, implanting a conductivity-enhancing dopant into the
10 semiconductor material to form graded junction regions operatively
11 adjacent the transistor gate. The invention also includes a
12 semiconductor transistor device comprising: a) a region of a
13 semiconductor material wafer; b) a transistor gate over a portion of the
14 region of the semiconductor material wafer, the transistor gate having
15 opposing lateral sidewalls; c) opposing source/drain regions operatively
16 adjacent the transistor gate, each source/drain region having an inner
17 lateral boundary; d) opposing sidewall spacers adjacent the sidewalls of
18 the transistor gate, each sidewall spacer having an outer lateral edge,
19 the sidewall spacers and source/drain regions being paired such that the
20 outer lateral edges of the sidewall spacers are displaced laterally
21 inwardly relative to the inner lateral boundaries of the source/drain
22 regions; and e) lateral gaps, the lateral gaps extending from the outer
23 lateral edges of the sidewall spacers to the inner lateral boundaries of
24 the source/drain regions.